PRODUCT SPECIFICATION

MODEL: MTF050FD55A-V1

<◇> PRELIMINARY SPECIFICATION

<◆> APPROVAL SPECIFICATION

CUSTOMER
APPROVED BY
DATE:

DESIGNED	CHECKED	APPROVED
LCM研发 2021.11.26 YYL	LCM研发 2021.11.26 YGP	LCM研发 2021.11.26 Edward

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Record of Revision

Rev	Issued Date	Description	Editor
V1	2021-11-26	Preliminary Specification Release	

1 General Specifications

Feature		Spec
Display Spec.	Size	5.0 inch
	Resolution	1080(RGB) x 1920
	Technology Type	LTPS
	Pixel Configuration	R.G.B. Vertical Stripe
	Pixel pitch(mm)	0.0191(W) * 0.0573(H)
	Display Mode	Normally Black
	LCM Luminance	350 Cd/m2
	Viewing Direction	ALL
Mechanical Characteristics	Module (W x H x D) (mm)	64.3x118.3x1.46±0.10mm
	Active Area(mm)	61.88x110.02mm
	Matching Connection Type	FPC
Electrical Characteristics	LED Numbers	12LEDs
	TFT Interface	MIPI
	Display color	16.7M
	LCD Driver IC	HX8399-C

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: /S0002

Note 3: LCM weight tolerance: 5

2 Input/Output Terminals

PinNo.	S	Description
1	IOVCC	Power supply for I/O
2	LEDPWM	PWM output pin of Backlight control.
3	DSWAP[1]	LNSW1/0 control swapping MIPI Lane
4	DSWAP[0]	LNSW1/0 control swapping MIPI Lane
5	PNSWAP	PNSW control Polarity of MIPI Pin
6	IM2	Interface select signal.
7	IM1	
8	IM0	
9	FTE1	est pin.
10	TE	Tearing effect output signal.
11	CS	Chip select signal.Low: Select (Accessible)High: Not Select (Inaccessible)
12	DC	Command/data select signal.
13	SCL	A synchronous clock signal in MIPI DBI Type Cand I2C operation
14	SDO	A serial data output pin in MIPI DBI Type Coperation
15	SDI	A serial data input pin in MIPI Type C operation to input data
16	RESE	Reset signal pin
17	C(NC)	NO Connection
18	GND	Ground
19	DSI-D2P	MIPI data2 positive signal
20	DSI-D2N	MIPI data2 negative signal
21	GN	Ground
22	DSI-D1P	MIPI data1 positive signal
23	DSI-D1N	MIPI data1 negative signal
24	GND	Ground
25	DSI-CLK	MIPI clock positive signal
26	DSI-CLK	MIPI clock positive signal
27	GND	Ground
28	DSI-D0P	MIPI data0 positive signal
29	DSI-D0N	MIPI data0 negative signal
30	GND	Ground
31	DSI-D3P	MIPI data3 positive signal
32	DSI-D3N	MIPI data3 negative signal
33	GND	Ground
34	AVDD	Power supply to analog circuit
35	AVEE	Power supply to analog circuit.
36	N	NO Connection
37	N	NO Connection
38	LEDA	LED Backlight anode
39	LEDK	LED Backlight cathode

3 Absolute Maximum Ratings

(Ta=25℃)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply voltage for Analog		VSP	4.8	5.5	6.0	V	
		VSN	-4.8	-5.5	-6.0	V	
Power supply voltage for Logic		IOVCC	1.70	1.80	1.90	V	
Input signal voltage (RES)		V_{IL}	0	-	0.3* IOVCC	V	XRES
		V_{IH}	0.7* IOVCC	-	IOVCC	V	
Onput signal voltage (TE)		V_{OL}	0	-	0.2* IOVCC	V	TE
		V_{OH}	0.8* IOVCC	-	IOVCC	V	
Input signal voltage (DSI)	Low level	$V_{IL(DSI)}$	-50	-	550	mV	Low power receiver
	High level	$V_{IH(DSI)}$	880	-	1350	mV	
	Input voltage	V_{CMRX}	70	-	-	mV	High speed receiver
	Differential input low threshold	V_{IDTL}	-70	-	-	mV	
	Differential input high threshold	V_{IDTH}	-	-	70	mV	

Note: The recommended operating condition refers to a range in which operation of this product is guaranteed. Should this range is exceeded, the operation cannot be guaranteed even if the values may be with the absolute maximum ratings. Accordingly, please make sure that the module is used within this range

4 Electrical Characteristics

4.1 LCD characteristics

GND 0V,Ta 25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		IOVCC	1.70	1.8	1.9	V	
Power Supply Voltage		VSP(+5V)	4.8	5.5	6.0	V	
Power Supply Voltage		VSN(-5V)	-4.8	-5.5	-6.0		
Input Signal Voltage	High Level	VIH	0.7*IOVCC	-	IOVCC	V	
	Low Level	VIL	0	-	0.3*IOVCC	V	

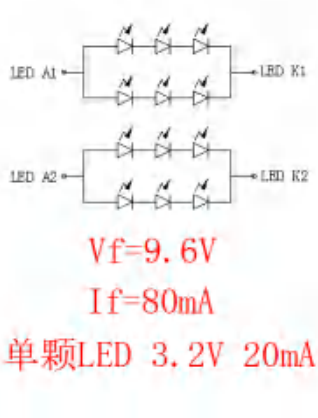
Table 4.1 LCD module electrical characteristics

4.2 Backlight Unit

Ta=25℃

Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	I_F	-	80	-	mA	12LEDs
Forward Voltage	V_F	-	9.6		V	BLH-BLL
Backlight Power Consumption	W_{BL}	-	768	-	mW	12LEDs
Operating Life Time	-	-	30,000	-	Hrs	For each LED

Note1: Figure below shows the connection of backlight LED.



Note 2: 1LED: V_F 6.0V I_F 20mA

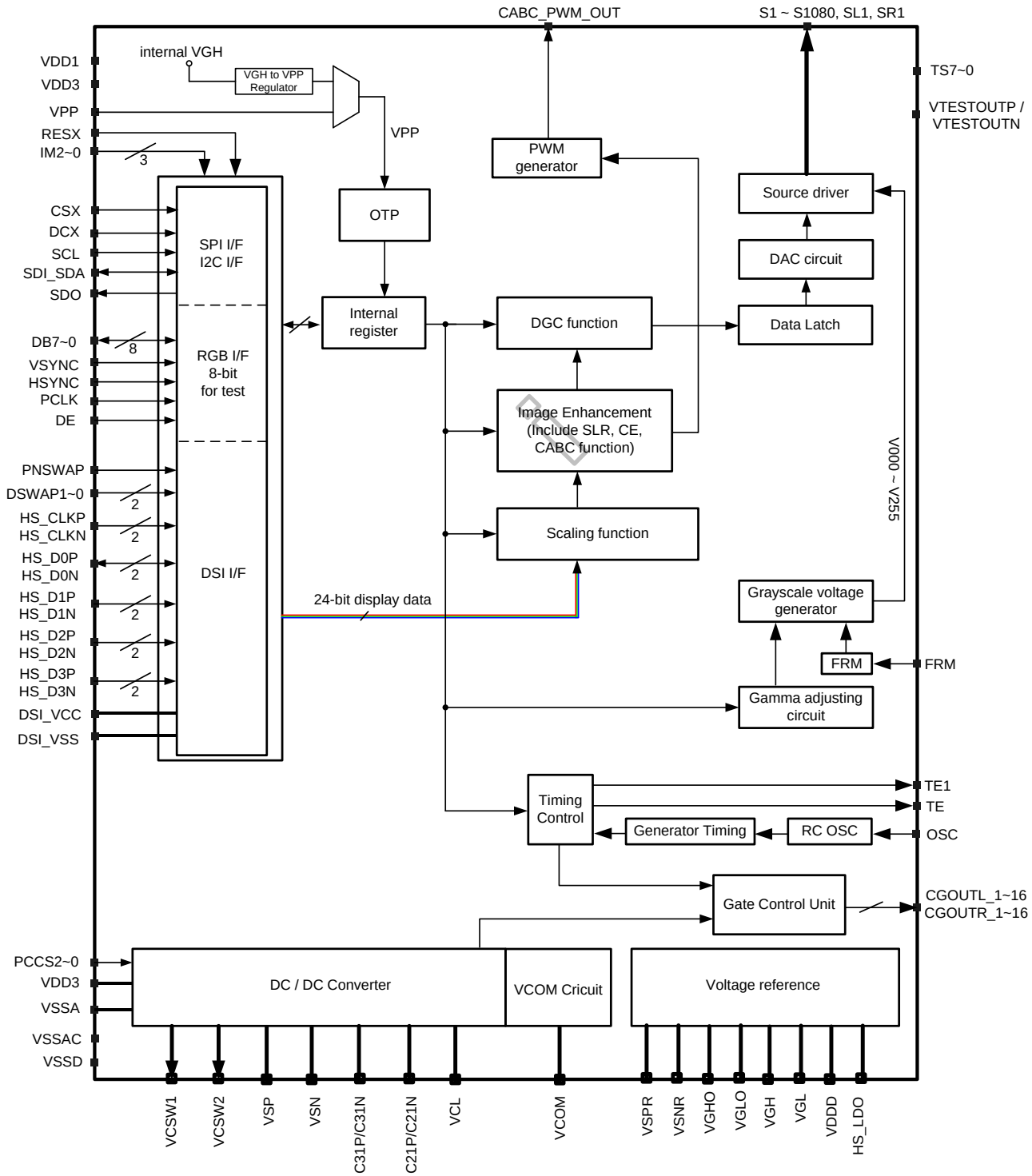
Note 3: I_F is defined for one LED.

Optical performance should be evaluated at Ta 25℃ only.

If LED is driven by high current, high ambient temperature humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50 initial brightness. Typical operating life time is estimated data.

5. Device Overview

5.1 Block diagram



5.2 Clock Lane Mode

Figure 4.13 shows the state diagram for Clock Lane Mode. The Clock Lane has three different power modes: Low Power Stop State, Ultra Low Power State **(ULPS)** and High Speed clock transmission.

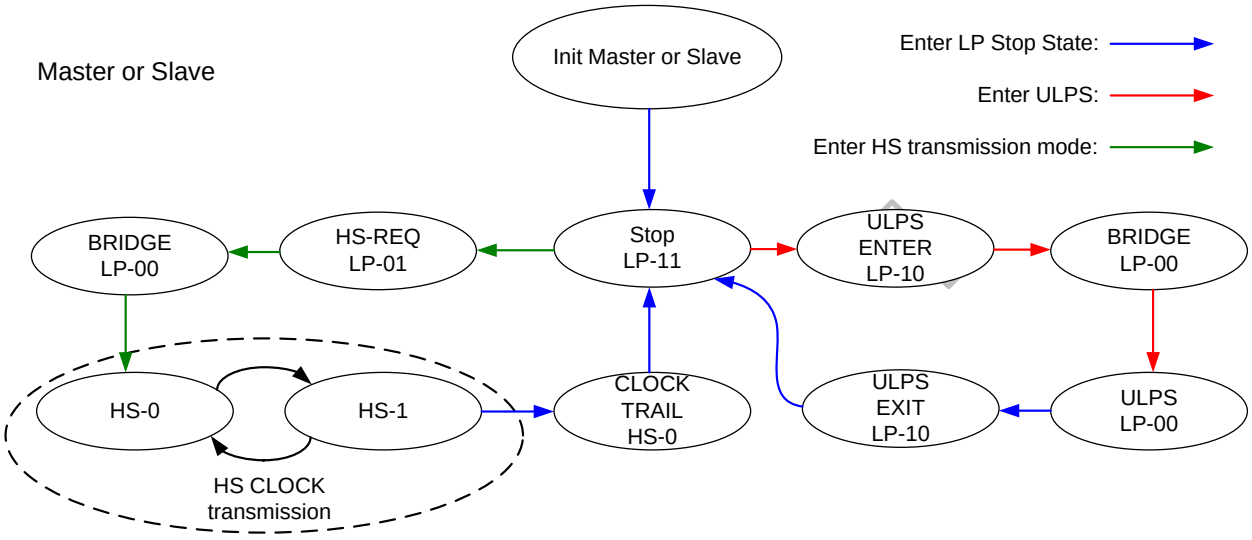
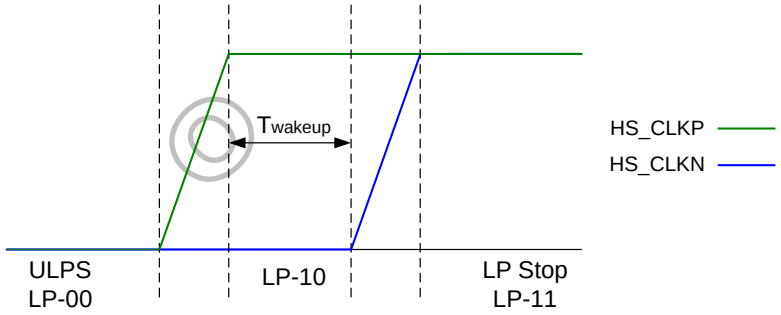


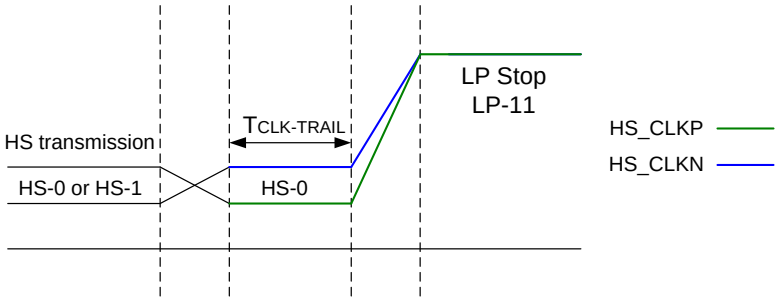
Figure 4.13: Clock Lane Mode State diagram

Clock Lane can be driven LP-11 to enter Low Power Stop State. There are three ways to enter Lower Power Stop State:

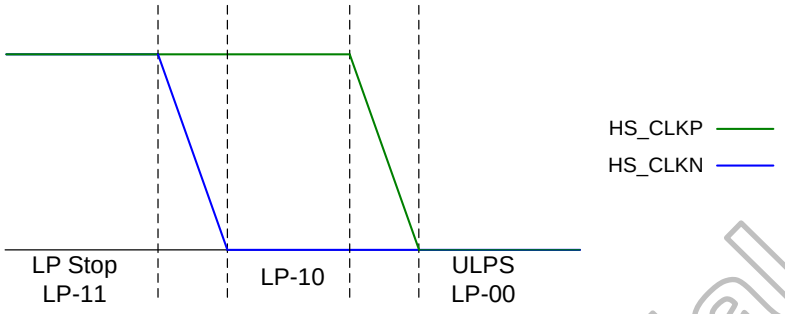
A. After Initial state **(HW reset, SW reset, Power on sequence)**.
B. Leaving ULPS: ULPS LP-00 → LP-10 → Low Power Stop State LP-11.



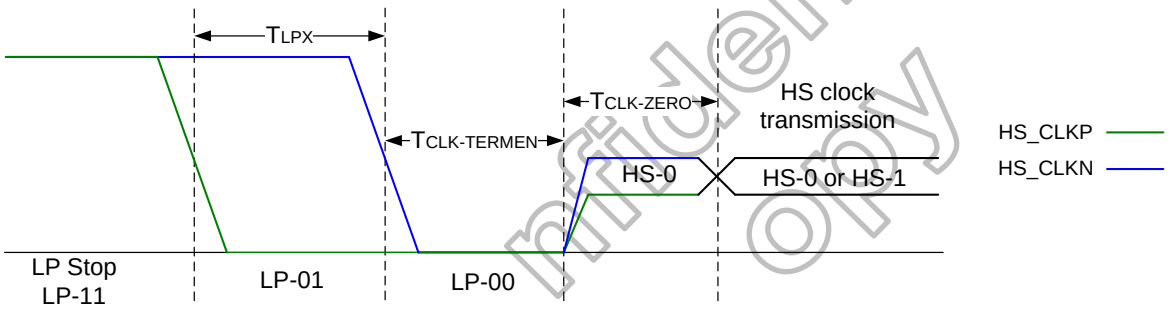
C. Leaving HS clock transmission mode: HS mode **(HS-0 or HS-1)** → HS-0 → Low Power Stop State LP-11.



Clock lane can be driven LP-00 to enter ultra low power state from low power stop state. The flow is low power stop state LP-11 → LP-10 → ULPS LP-00.



Clock lane can be high speed clock transmission state from low power stop state. The flow is low power stop state LP-11 → LP-01 → LP-00 → HS-0/1.



5.3 Data Lane Mode

Figure 4.14 shows the operational flow diagram for Data Lane Mode. There are three operating modes in Data Lane: Escape mode, High-Speed transmission mode and Turnaround.

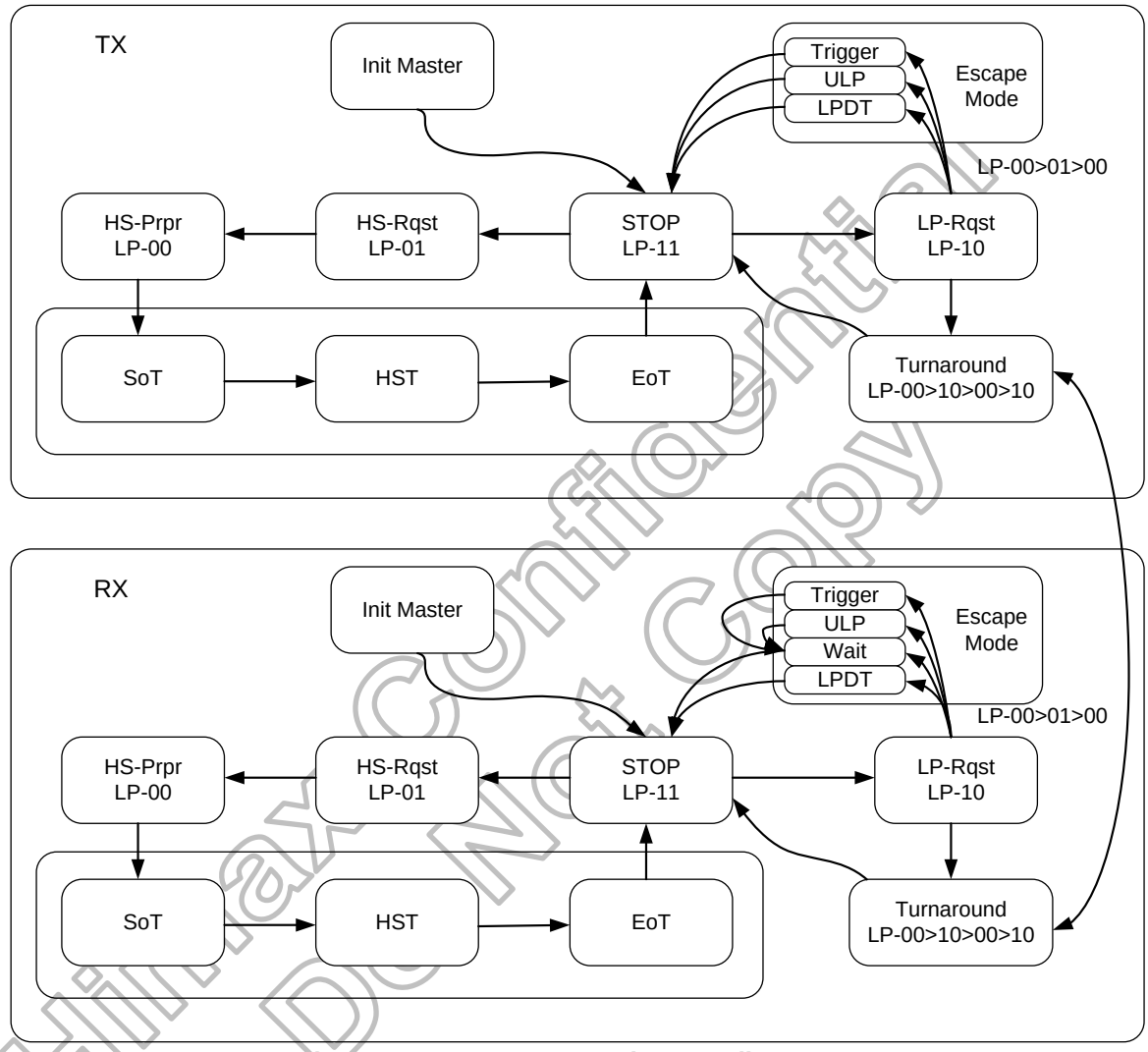


Figure 4.14: Data Lane Mode State diagram

5.4 High speed data transmission

The display module can enter High Speed Data Transmission when Clock Lane in the High Speed Clock Mode. All Data Lane enter High Speed Data Transmission synchronously but may end at different time. Data Lane enters High Speed Data Transmission by the flow: LP-11 → LP-01 → LP-00→ SoT**(HS-00011101)**. And exit High Speed Data Transmission flow: Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$.

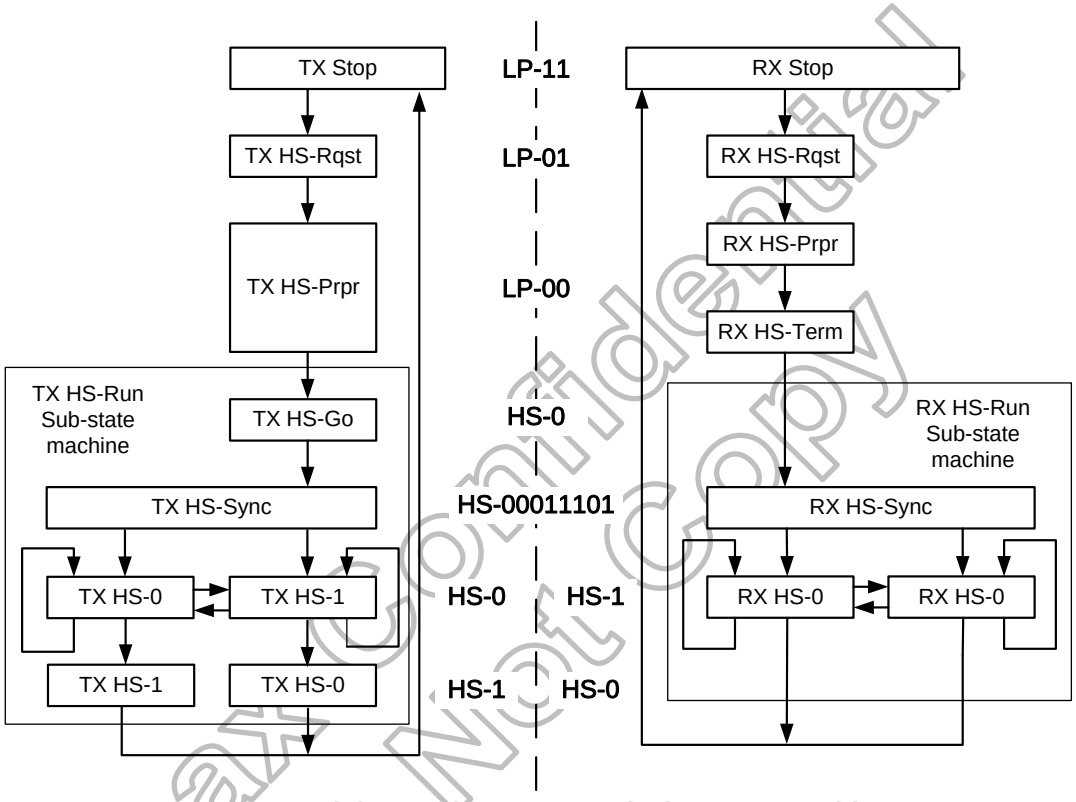


Figure 4.17: High Speed Data Transmission State Machine

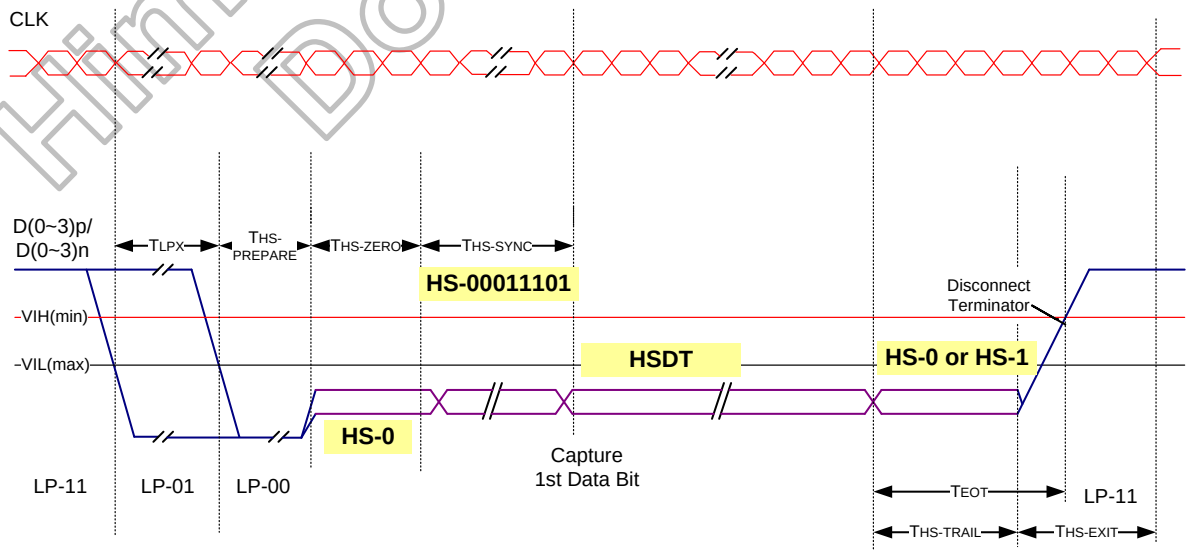


Figure 4.18: High Speed Data Transmission timing sequence

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	40+4*UI	-	85+6*UI	ns
$T_{HS-PREPARE}$+ $T_{HS-ZERO}$	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145+10*UI	-	-	ns
T_{EOT}	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.	-	-	105ns+12*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	60ns+4*UI	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Table 4.4: Global operation timing parameters for data lane

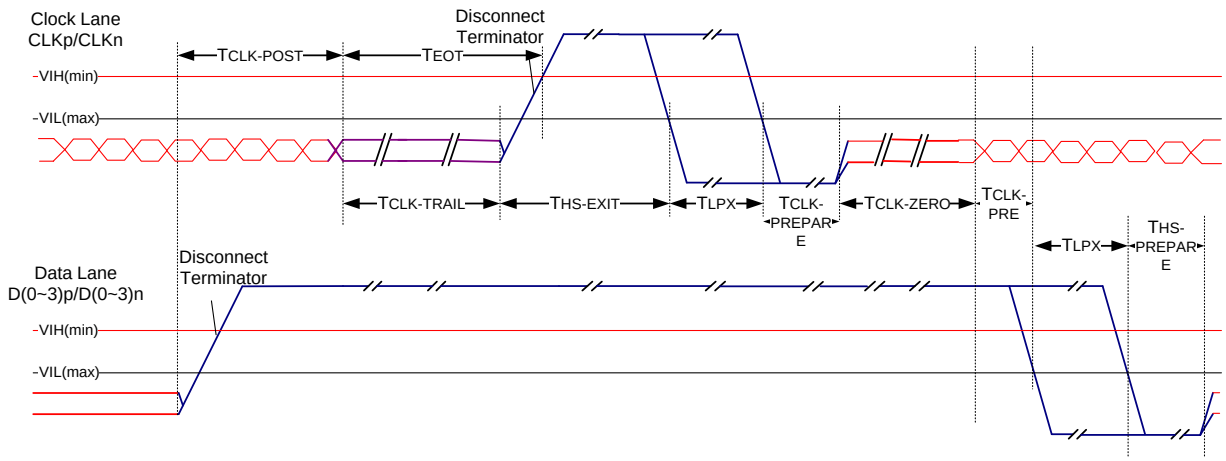


Figure 4.19: Switching the clock lane between clock transmission and LP mode

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60+52*UI	-	-	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	60	-	-	ns
$T_{CLK-PREPARE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	38	-	95	ns
$T_{CLK-PREPARE+}$ $T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns

Table 4.5: Global operation timing parameters for clock lane

6.1 VDD3/VDD1

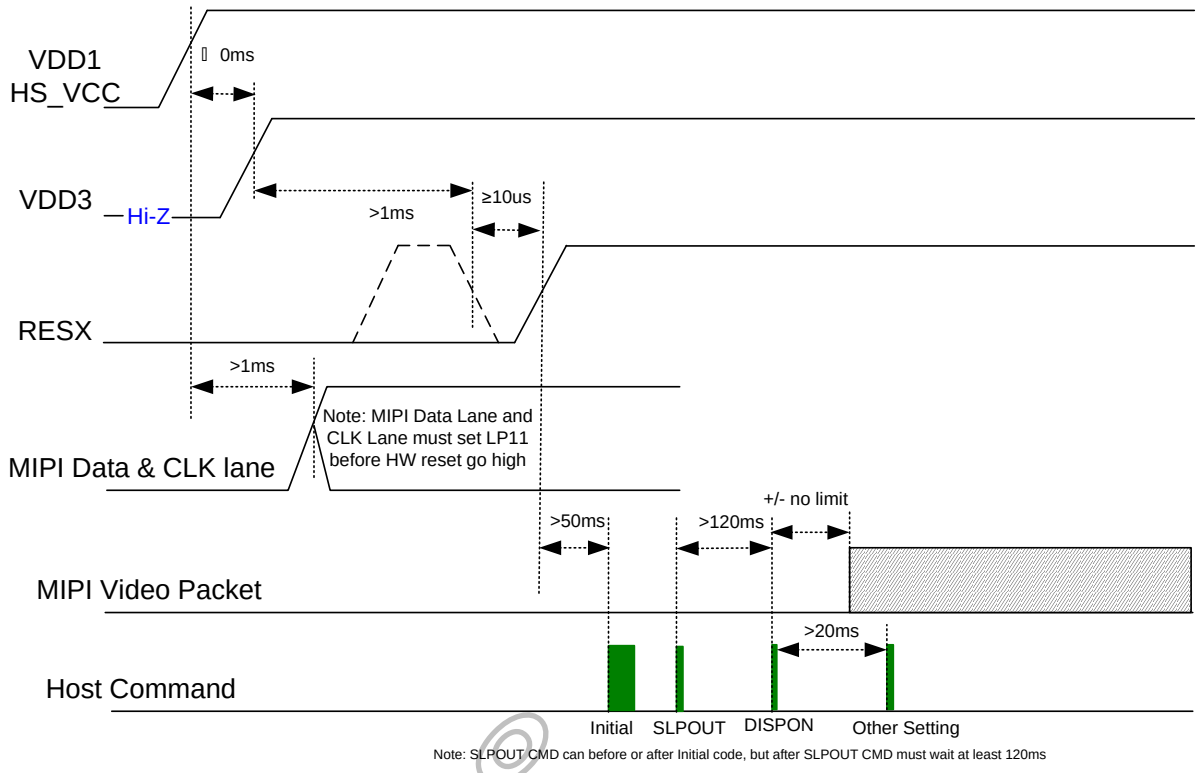


Figure 5.30: VDD3/VDD1 input power on sequence (PCCS[2:0]=000/001/101)

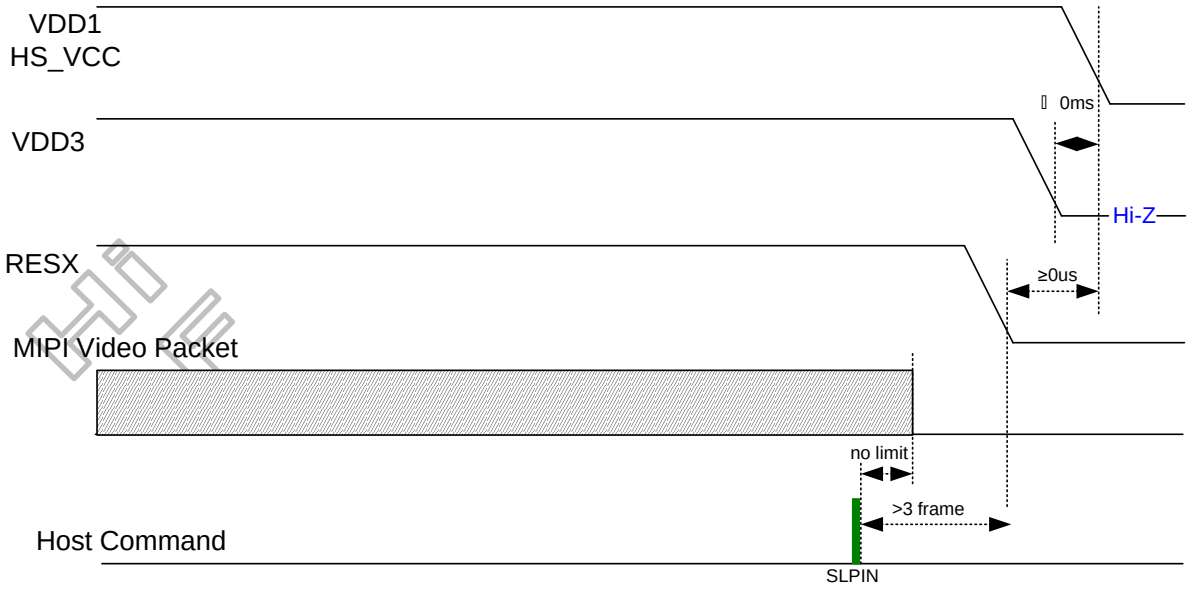


Figure 5.31: VDD3/VDD1 input power off sequence (PCCS[2:0] =000/001/101)

6.2 VSP/VDD1 input power (PCCS[2:0]=010)

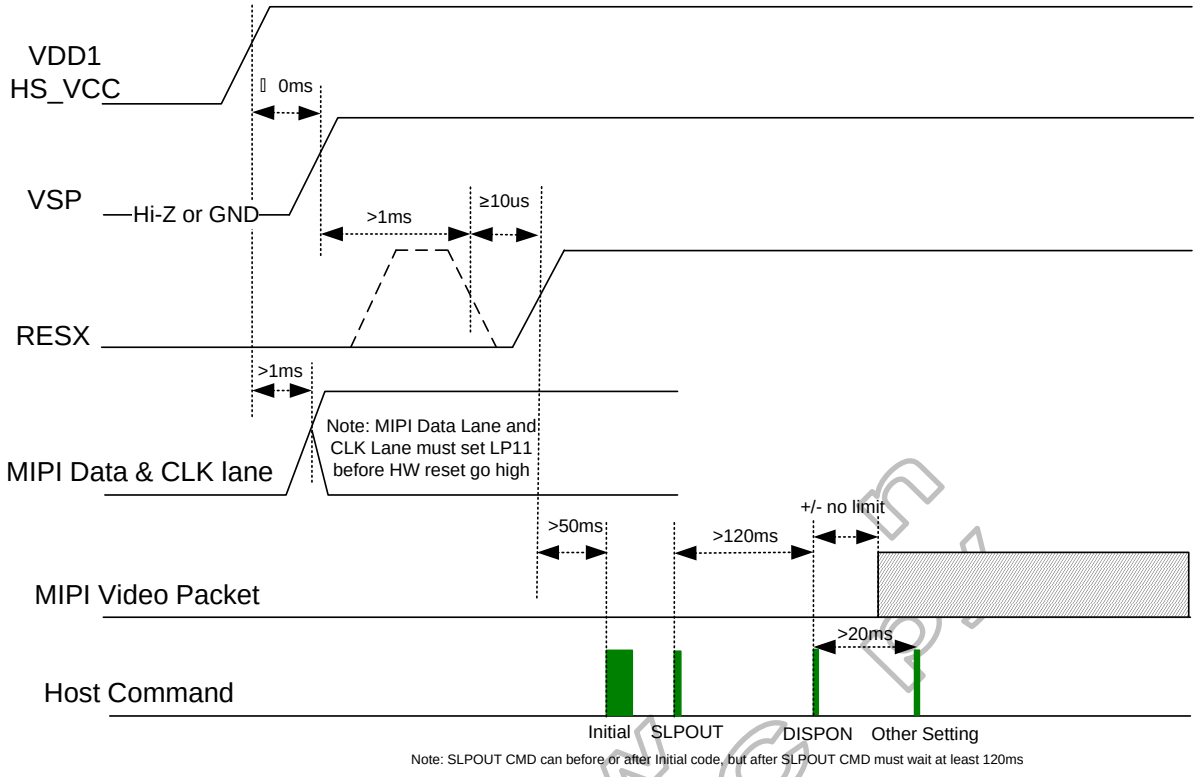


Figure 5.32: VSP/VDD1 input power on sequence (PCCS[2:0] =010)

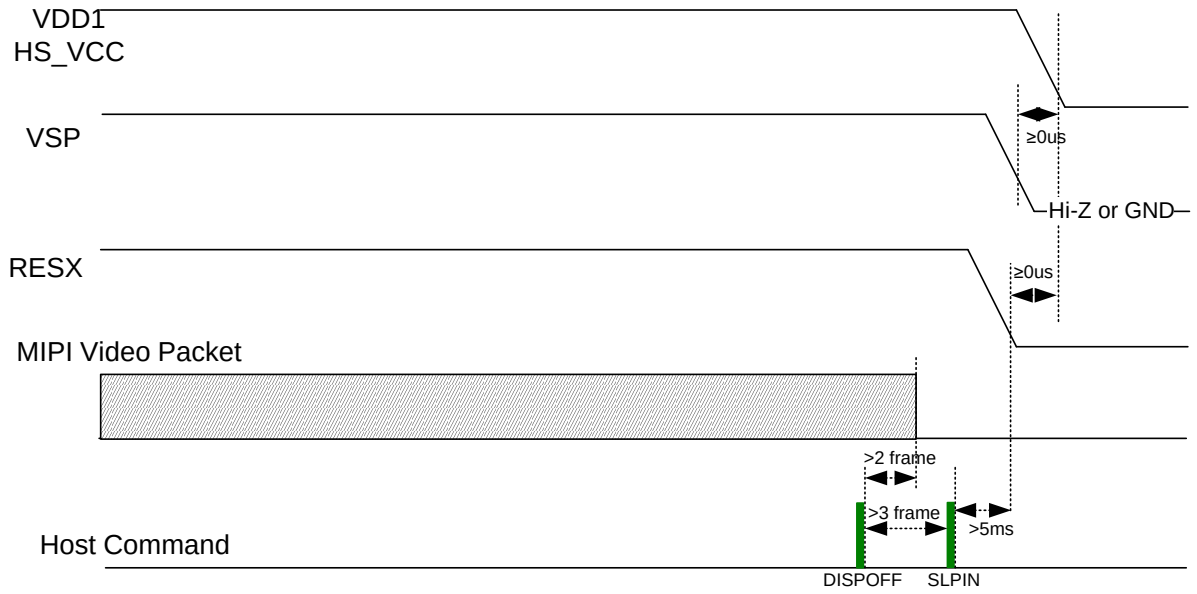


Figure 5.33: VSP/VDD1 input power off sequence (PCCS[2:0] =010)

6.3 VSP/VSN/VDD1 input power (PCCS[2:0]=011)

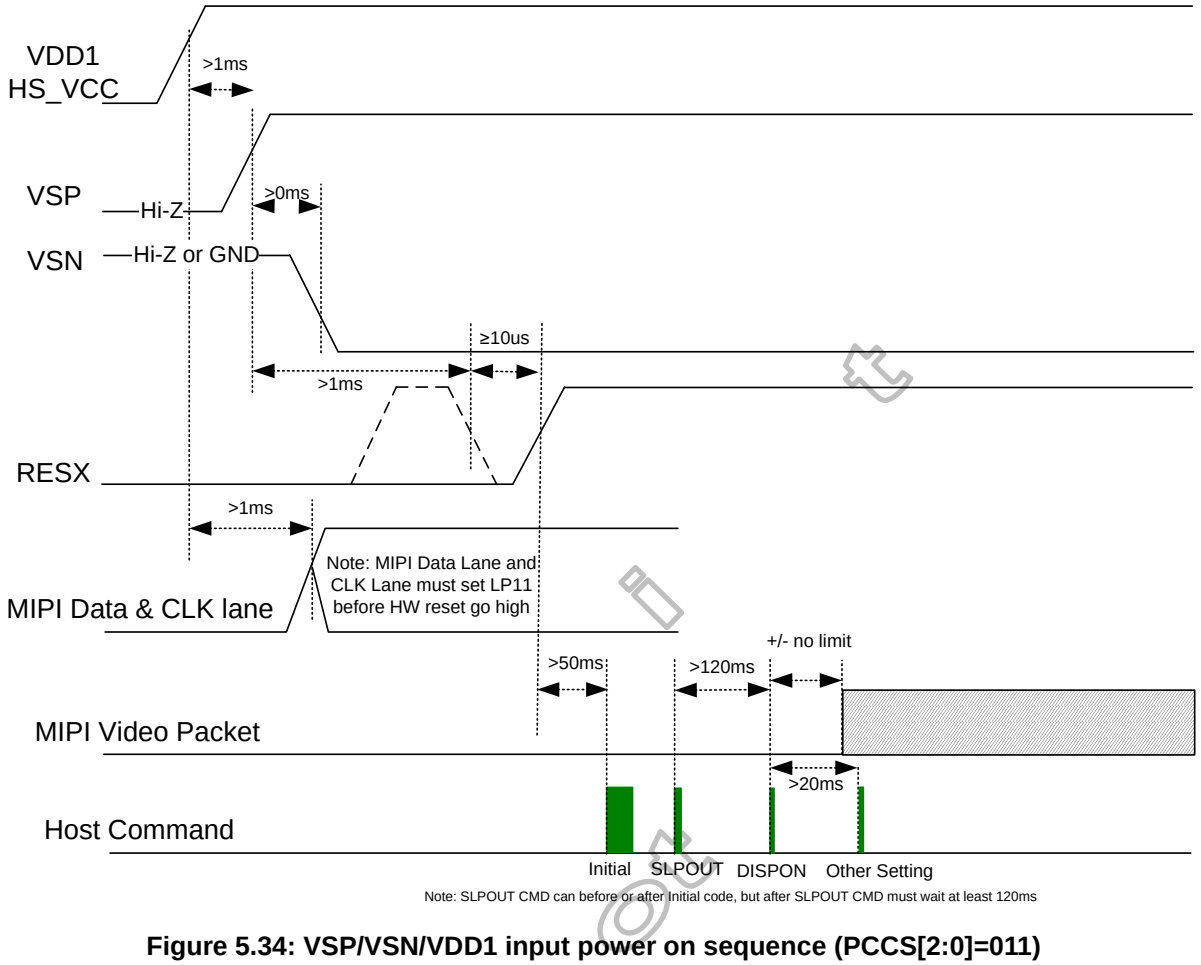


Figure 5.34: VSP/VSN/VDD1 input power on sequence (PCCS[2:0]=011)

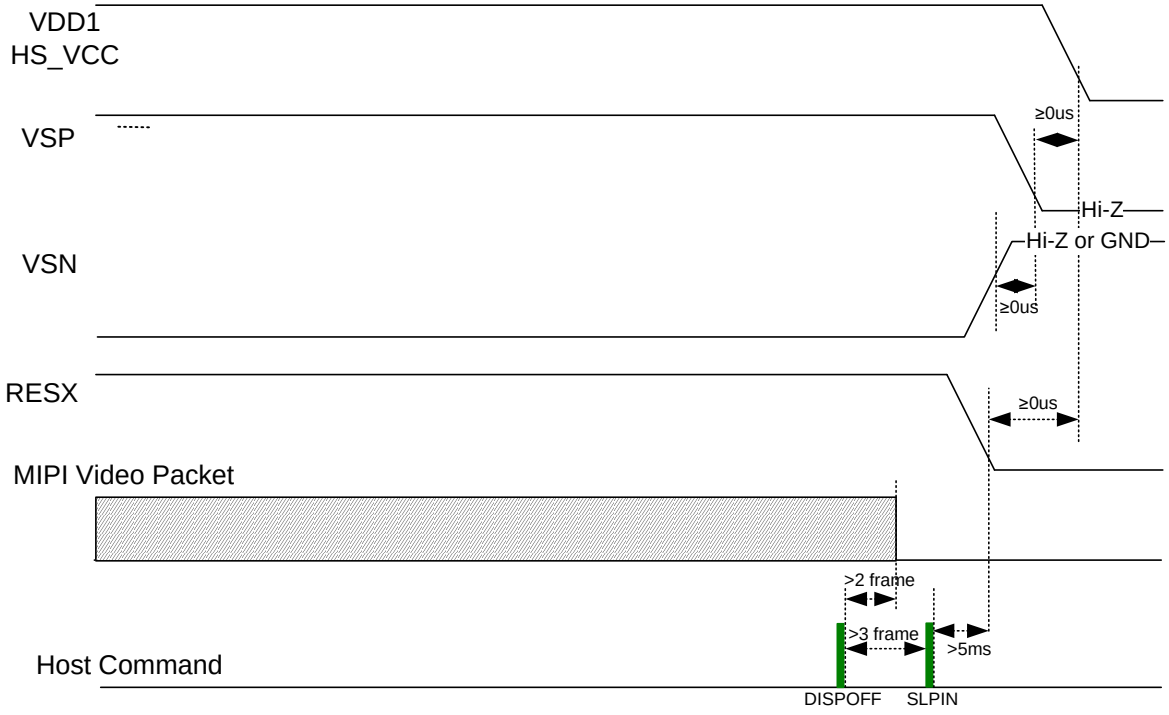


Figure 5.35: VSP/VSN/VDD1 input power off sequence (PCCS[2:0]=011)

6.4 VDD3/VSP/VSN/VDD1 input power (PCCS[2:0]=111)

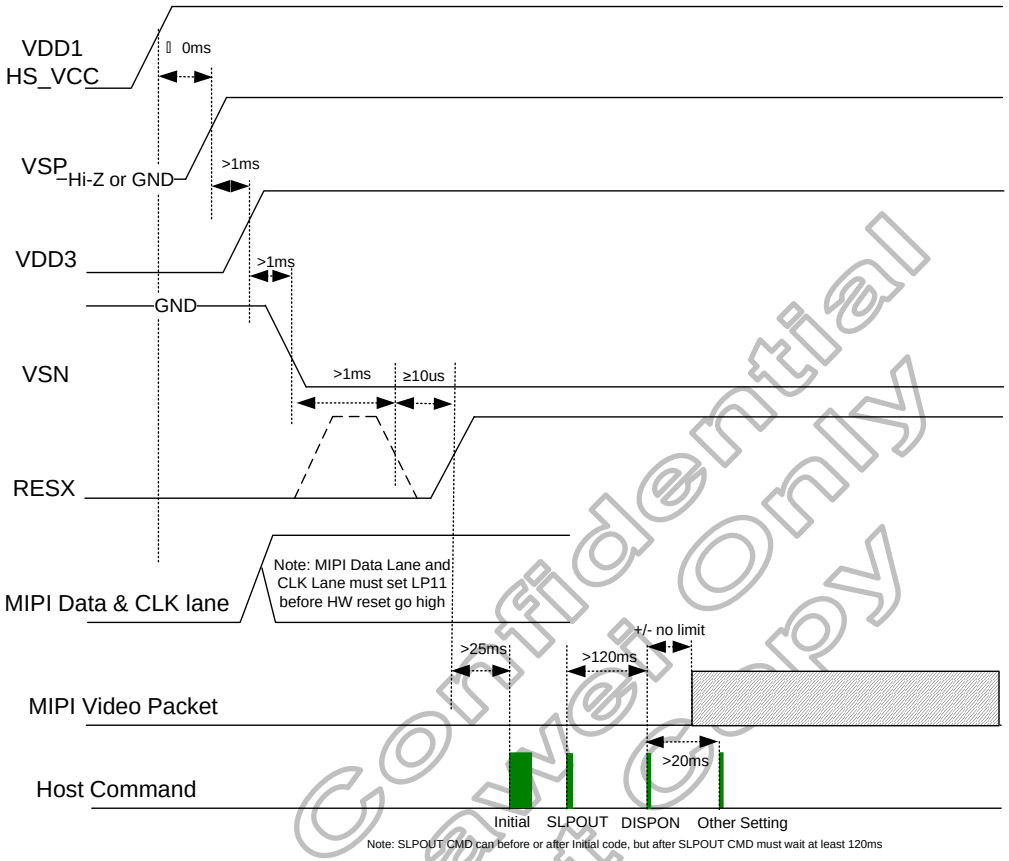


Figure 5.36: VDD3/VSP/VSN/VDD1 input power on sequence (PCCS[2:0]=111)

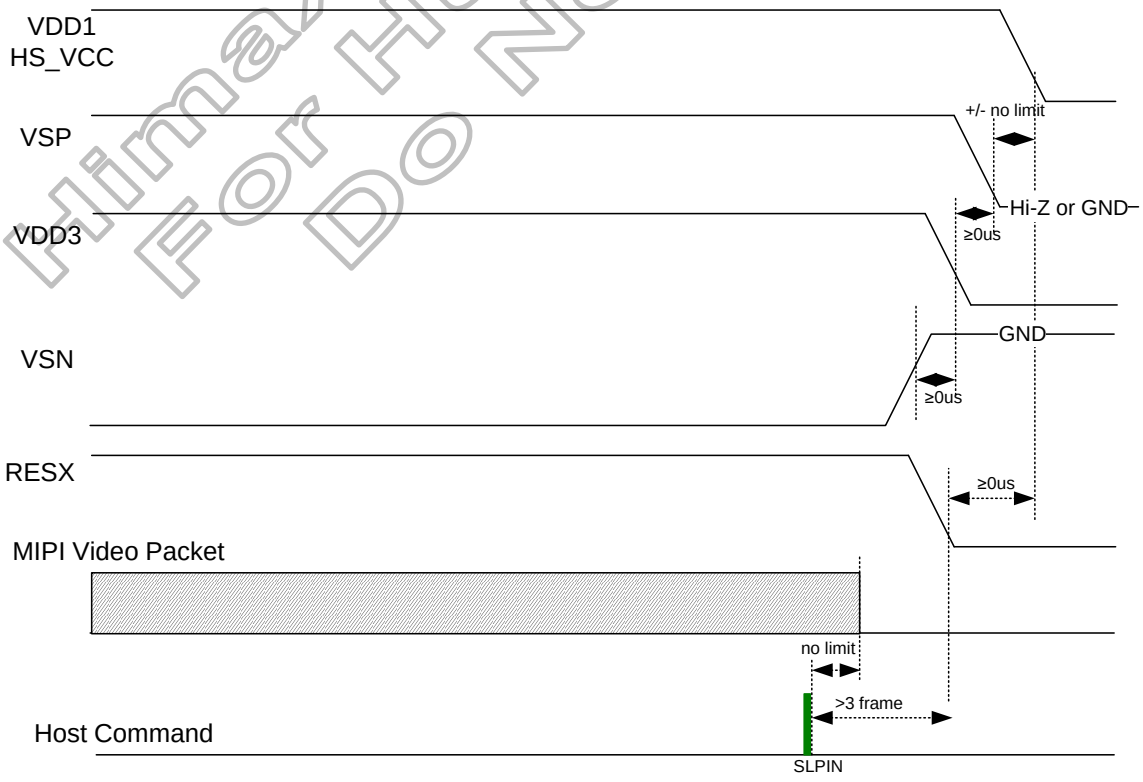


Figure 5.37: VDD3/VSP/VSN/VDD1 input power off sequence

6.5 VSP/VSN/VGH/VGL/VDD1 input power (PCCS[2:0]=100)

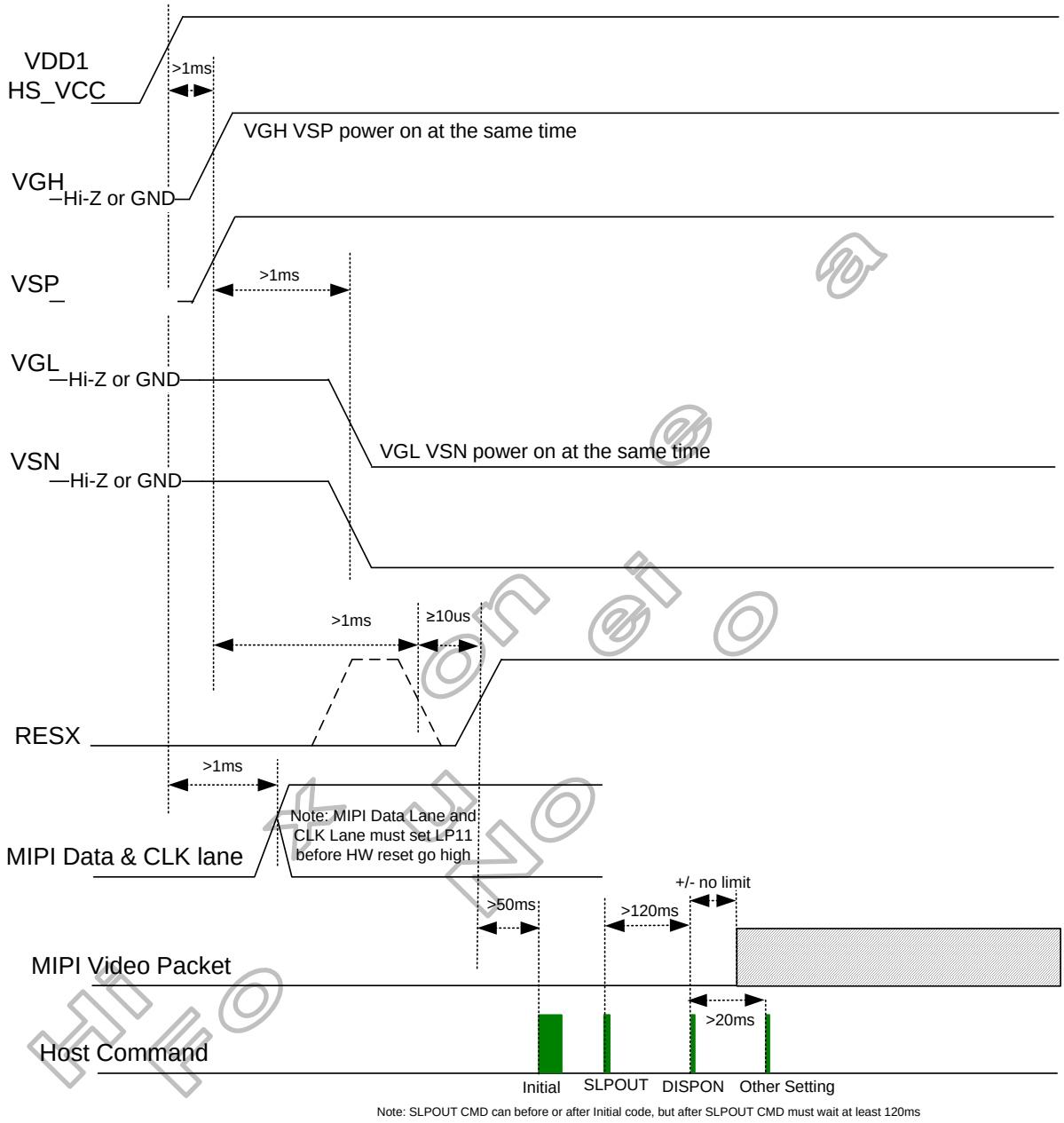


Figure 5.38: VSP/VSN/VGH/VGL/VDD1 input power on sequence

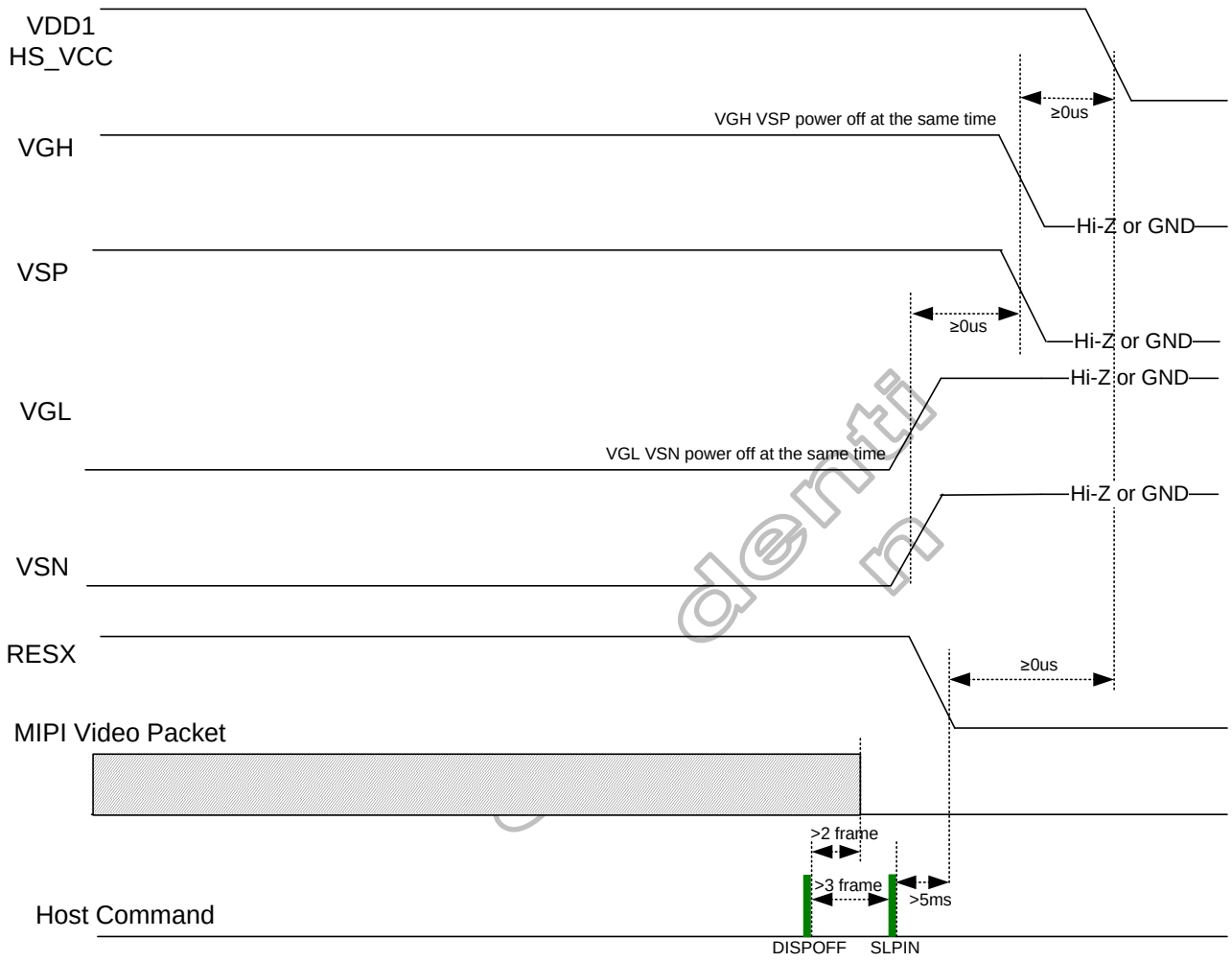


Figure 5.39: VSP/VSN/VGH/VGL/VDD1 input power off sequence

7 Optical Characteristics

7.1 Driving the backlight condition

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ3	CR>10	70	80	-	Deg.	Note1
		Θ9		70	80	-	Deg.	
	Vertical	Θ12		70	80	-	Deg.	
		Θ6		70	80	-	Deg.	
Contrast ratio		CR	Θ = 0°	1000	1500	-		Note2
Transmittance		Tr		3.6	4.3		%	Note3
Color Gamut		CG	CIE1931	55	60		%	NTSC
Reproduction of color	Red	Rx	Θ = 0°	0.602	0.632	0.662		Note4 (Based on C Light)
		Ry		0.283	0.313	0.343		
	Green	Gx		0.272	0.302	0.332		
		Gy		0.567	0.597	0.627		
	Blue	Bx		0.113	0.143	0.173		
		By		0.107	0.137	0.167		

*Note (1) Definition of Contrast Ratio (CR):

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
White Chromaticity	Wx	Θ = 0°	0.270	0.300	0.330		Note 4
	Wy		0.308	0.338	0.368		
Response Time (Rising + Falling)	$T_r + T_f$	Ta= 25° C Θ = 0°	-	-	35	ms	Note 5

7 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	**Ts=+70℃, 24hrs Restore 2H at 25℃ Power off**	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	**Ta=-20℃, 24hrs Restore 2H at 25℃ Power off**	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	**Ta=+70℃, 24hrs Restore 2H at 25℃ Power off**	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	**Ta=-20℃, 24hrs Restore 2H at 25℃ Power off**	IEC60068-2-1:2007 GB2423.1-2008
5	Storage at High Temperature and Humidity	**Ta=+60℃, 90% RH, 24 hours Restore 2H at 25℃ Power off**	IEC60068-2-78 :2001 GB/T2423.3 2006
7	ESD Sensitivity test	**C=150pF, R=330Ω,5points/ panel Air:± 6KV, 5times, Contact:± 4KV, 5 times, （Environment: 15℃～35℃, 30%～60%, 86Kpa～106Kpa）**	IEC61000-4-2:2001 GB/T17626.2-2006

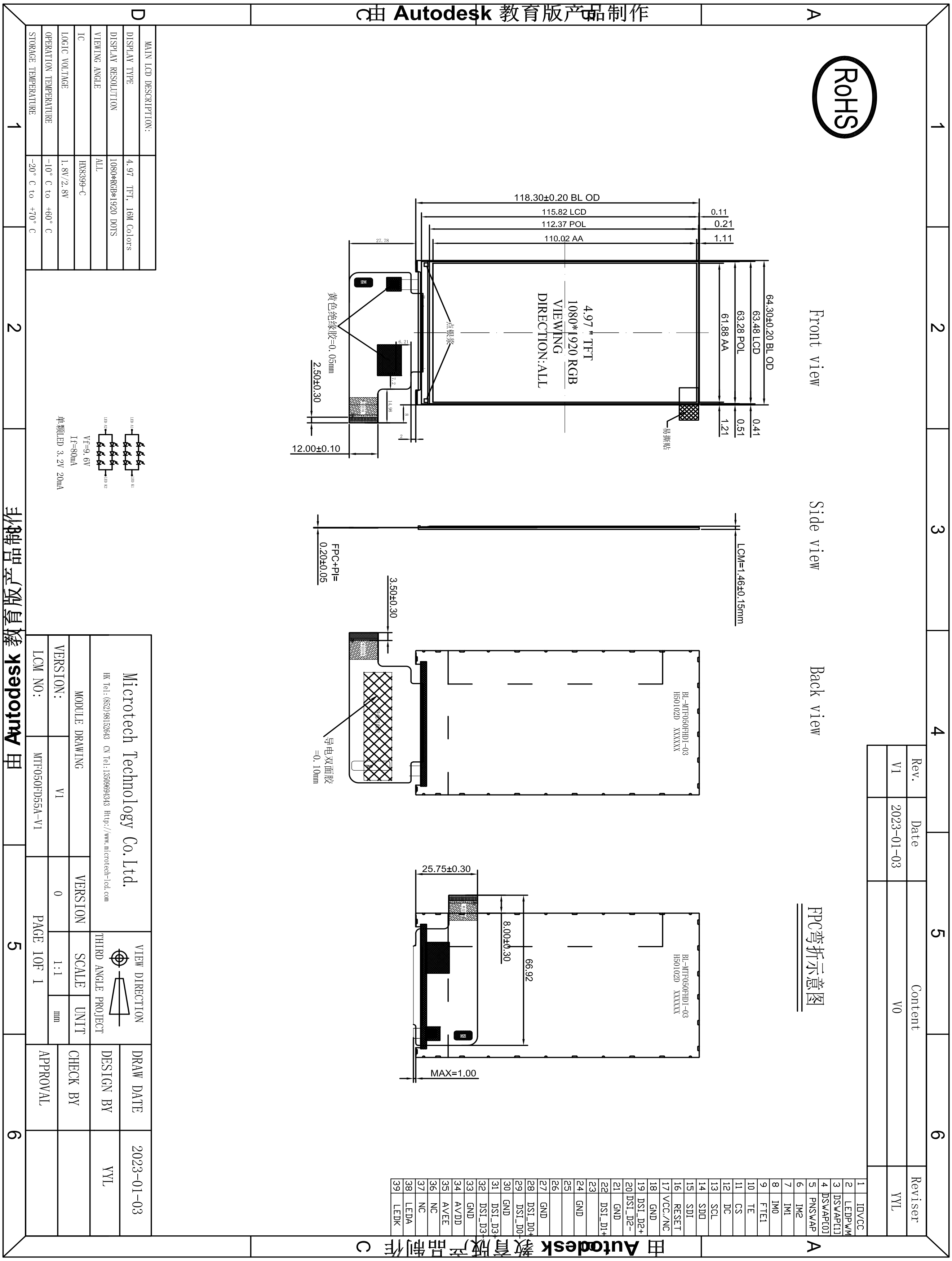
Note1: Ts is the temperature of panel s surface.

Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don t guarantee all of the cosmetic specification.

8 Mechanical Drawing


由 Autodesk 教育版产品制作
MAIN LCD DESCRIPTION:
DISPLAY TYPE 4.97 TFT, 16M Colors
DISPLAY RESOLUTION 1080*RGB*1920 DOTS
VIEWING ANGLE ALL
IC HX8399-C
LOGIC VOLTAGE 1.8V/2.8V
OPERATION TEMPERATURE -10° C to +60° C
STORAGE TEMPERATURE -20° C to +70° C
RoHS
Front view
Side view
Back view
FPC弯折示意图
4.97" TFT
1080*1920 RGB
VIEWING
DIRECTION:ALL
118.30±0.20 BL OD
115.82 LCD
112.37 POL
110.02 AA
64.30±0.20 BL OD
63.48 LCD
63.28 POL
61.88 AA
12.00±0.10
2.50±0.30
LCM=1.46±0.15mm
FPC+PI=0.20±0.05
3.50±0.30
25.75±0.30
8.00±0.30
66.92
MAX=1.00
BL-MTF050FHD1-03
H50102D XXXXXX
Vf=9.6V
If=80mA
单颗LED 3.2V 20mA
Microtech Technology Co.Ltd.
MODULE DRAWING
VERSION: V1
LCM NO: MTF050FD55A-V1
VERSION 0
SCALE 1:1
UNIT mm
PAGE 1OF 1
VIEW DIRECTION
THIRD ANGLE PROJECT
DRAW DATE 2023-01-03
DESIGN BY YYL
CHECK BY
APPROVAL
Rev. V1
Date 2023-01-03
Content V0
Reviser YYL
1 IOVCC
2 LEDPWM
3 DSWAP[1]
4 DSWAP[0]
5 PNSWAP
6 IM2
7 IM1
8 IM0
9 FTE1
10 TE
11 CS
12 DC
13 SCL
14 SDO
15 SDI
16 RESET
17 VCC/NC
18 GND
19 DSI_D2+
20 DSI_D2-
21 GND
22 DSI_D1+
24 GND
27 GND
28 DSI_D0+
29 DSI_D0-
30 GND
32 DSI_D3-
33 GND
34 AVDD
35 AVEE
36 NC
37 NC
38 LEDA
39 LEDK

9 Packing Drawing

No.	Item	Model (Material)	Dimensions(mm)	Unit Weight (kg)	Quantity	Remark
1	LCM Module	MTF050FD55A-V1	65.30x119.3x1.85mm	TBD	TBD	
2	Partition	BC Corrugated paper	TBD	TBD	TBD	
3	Corrugated Paper	B Corrugated paper	TBD	TBD	TBD	
4	Corrugated Bar	B Corrugated paper	TBD	TBD	TBD	
5	Dust-Proof Bag	PE	TBD	TBD	TBD	
6	A/S Bag	PE	TBD	TBD	TBD	
7	Carton	Corrugated paper	TBD	TBD	TBD	
8	Total weight	TBD Kg±5%				

10 Precautions for Use of LCD Modules

10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not sub ect it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the ad oining areas since this may cause the color tone to vary.

10.1.4 The polari er covering the display surface of the LCD module is soft and easily scratched. Handle this polari er carefully.

10.1.5 If the display surface is contaMinated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polari er. Especially, do not use the following:

- Water
- etone
- Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage precautions

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

10.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.